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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,327	08/19/2003	Jean Khawand	CE11193JI210	4001

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EXAMINER	
NGUYEN, MIKE	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,327	KHAWAND ET AL.	
	Examiner	Art Unit	
	Mike Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/09/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notices & Remarks

1. Applicant's amendment 06/09/2005 in response to Examiner's Office Action has been reviewed. The following rejections now apply.

2. Claims 1-19 are pending for the examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9 and 11-19 are rejected under 35 U.S.C. 102(b) as being anticipated by (U.S. Pat. No. 6,388,989 B1).

As to claim 1, Malhotra teaches an electronic device (fig. 1), comprising:

a first processor (CPU 18 of fig. 1);

a second processor coupled to the first processor (HDLC controller 12);

shared memory coupled to the first and second processors (shared memory 20 of fig. 1); and

wherein the first processor manages the shared memory and allocates a message buffer to the second processor whenever the second processor needs to send a message to the first processor, and wherein the first processor sends a message buffer pointer to the second processor that directs the second processor to the message buffer (col. 4 line 51 to col. 5 line 11).

As to claim 2, Malhotra teaches an electronic device as defined in claim 1, wherein the first processor sends the message buffer pointer to the second processor in response to receiving an empty buffer request from the second processor (col. 4 line 61 col. 5 line 1).

As to claim 3, Malhotra teaches an electronic device as defined in claim 2, wherein after receiving the message buffer pointer the second processor fills the message buffer with the message (col. 5 lines 2-4).

As to claim 4, Malhotra teaches an electronic device as defined in claim 3, wherein after filling up the message buffer with the message, the second processor passes the message buffer pointer to the first processor (col. 5 lines 5-11).

As to claim 5, Malhotra teaches an electronic device as defined in claim 4, wherein the first processor reads the message from the message buffer after receiving the message buffer pointer (col. 5 lines 2-4).

As to claim 6, Malhotra teaches an electronic device as defined in claim 5, wherein after reading the message, the first processor releases the message buffer (col. 5 lines 5-8).

As t o claim 7, Malhotra teaches an electronic device as defined in claim 1, wherein a plurality of buffers assigned to the second processor are located in the shared memory (buffers 142 and 146 of fig. 4).

As to claim 8, Malhotra teaches an electronic device as defined in claim 7, wherein the plurality of buffers assigned to the second processor are used by the second processor without having to request them from the first processor (col. 4 lines 14-21).

As to claim 9, Malhotra teaches an electronic device as defined in claim 8, wherein when the second processor needs to send a message to the first processor it loads a starting address of the message in one of the plurality of buffers assigned to the second processor (col. 4 line 66 to col. 5 line 11).

As to claim 11, Malhotra teaches a method for providing interprocessor communication between first and second processors using a shared memory (CPU 18, HDLC controller 12 and shared memory 20 of fig. 1), the first processor assigned to manage the shared memory, the method comprising the steps of:

(a) sending a request from the second processor requesting an empty message buffer from the shared memory when the second processor needs to send a message to the first processor (col. 4 lines 44-53);

(b) sending a message buffer pointer from the first processor to the second processor in response to the request in step (a) (col. 5 line 61 to col. 5 line 11);

(c) using the message buffer pointer by the second processor to the second processor to locate the empty message buffer in the shared memory wherein the message is going to be loaded (col. 4 line 61 to col. 5 line 4); and

(d) loading the empty message buffer with message (col. 5 lines 2-4).

As to claim 12, Malhotra teaches a method as defined in claim 11, further comprising the step of:

(e) sending the message buffer pointer back to the first processor (col. 5 lines 5-11).

As to claim 13, Malhotra teaches a method as defined in claim 12, wherein in response to step (e) the first processor performs the step of:

(f) reading the message (col. 5 lines 2-4).

As to claim 14, Malhotra teaches a method as defined in claim 13, further comprising the step of:

(g) releasing the empty message buffer once step (f) has been performed (col. 5 lines 5-8).

As to claim 15, Malhotra teaches a method for providing interprocessor communication between first and second processors using a shared memory (CPU 18, HDLC controller 12 and shared memory 20 of fig. 1), the first processor assigned to manage the shared memory, the method comprising the steps of:

at the first processor:

(a) allocating a memory buffer from the shared memory for use in loading a message to be sent to the second processor (col. 4 line 61 to col. 5 line 1);

(b) loading the message in the memory buffer (col. 5 lines 2-4);

(c) sending a message buffer pointer to the second processor (col. 5 line 61 to col. 5 line 11); and

at the second processor:

(d) using the message buffer pointer to locate the message in the shared memory (col. 4 line 61 to col. 5 line 4).

As to claim 16, Malhotra teaches a method as defined in claim 15, further comprising the step of at the second processor: (e) reading the message; and (f) sending the message buffer pointer back to the first processor (col. 5 lines 2-11).

As to claim 17, Malhotra teaches a method as defined in claim 16, wherein the first processor upon receiving the message buffer pointer in step (f), release the allocated memory buffer so it can be used for a future message (col. 5 lines 5-8).

As to claim 18, Malhotra teaches a method as defined in claim 15, wherein step (c) is performed by the first processor sending the starting address of the allocated memory buffer to a memory located in the second processor (col. 4 line 66 to col. 5 line 1).

As to claim 19, Malhotra teaches a method as defined in claim 18, wherein the first processor sends an interrupt to the second processor once it has loaded the starting address of the allocated memory buffer in the memory located in the second processor (col. 5 lines 2-11).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Malhotra in view of Baumgartner (U.S. Pat. No. 6,507,760 B1).

As to claim 10, Malhotra fails to explicitly teach a radio communication device. Baumgartner; however, teaches the radio communication device (fig 1). It would have been obvious to a person of ordinary skill in the art to have the radio communication device in order to provide communication between the electronic device having multiprocessor with other devices.

Response to Arguments

7. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is 571 272-4153. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on 571 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Nguyen
Patent Examiner
Group Art Unit 2182

08/10/2005

KIM HUYNH
PRIMARY EXAMINER
8/11/05